REMARKS

Applicant appreciates Examiner's thorough review of the application.

Reconsideration and allowance of all claims are requested.

Claims 1 - 4 are patentable under 35 U.S.C. 103(a) over Jewett et al. (US No. 6,263,452) in view of Abbondanzio et al. (US No. 6,931,568).

Claims 1 - 4 are patentable over Jewett et al. (US No. 6,263,452) in view of Abbondanzio et al. (US No. 6,931,568) because neither reference teaches or suggests all of the limitations of any of the claims. Claim 1 teaches that "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." No reference teaches or suggests this simple way of restoring a system, which is an important feature of the present invention.

Jewett teaches a computer system with multiple, identical CPUs and memory modules. Jewett's CPUs are loosely synchronized and execute the same instruction stream and its memory modules store duplicates of the same data. The system detects faults in the CPUs and memory modules and places a faulty unit offline for replacement while continuing operation. (See Abstract) However, Jewett requires numerous complicated steps to restore its system after a fault, such as determining status, selective shut off of the I/O processors, issuing a reset command to the shut off processor, etc. (See Col. 27, lines 5 - 48). Jewett does not teach "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again."

Abbondanzio is a method for determining an active service processor from redundant service processors in a system. A control logic is used to receive status signals from the service processor and use them to generate a control signal. A management module control logic maintains the control signal in its present state while the active processor is functional, but alters the control signal if the active service processor is non-functional, causing managed subsystems to switch over to an inactive or standby service processor to receive service processor signals. (See Abstract)

Abbondanzio does not teach "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." Examiner cites to Col. 10, lines 3-47 as teaching this feature, however that section of the reference does not teach such a feature and does not refer at all to attaching or detaching a CPU board.

Abbondanzio teaches that a watchdog timer may be used to reset the local service processor if the processor "hangs." (Col. 2, lines 30-32). Thus Abbandanzio teaches away from restoring the system by "detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." Abbandanzio teaches that when a processor hangs, it should be electronically reset using a watchdog timer. The present invention does not require a watchdog timer or electronic resetting. Resetting is very different from actually detaching and reattaching a CPU board.

Therefore, no reference teaches or suggests "if one of the CPU boards is down, the system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." For at least that reason, the rejection of Claim 1 under 35 U.S.C. 103(a) is

improper and should be withdrawn. Claims 2 and 3 depend on Claim 1 and therefore should be allowed as well.

Claim 2 adds the patentable feature that "if one of the CPU boards or power sources is down, the system is restored by detaching said down CPU board or said down power source from said bus and attaching said detached CPU board or said detached power source to said bus again." For the same reasons as discussed above, no reference teaches or suggests this feature. Examiner additionally cites to Col. 4, lines 49-65 as teaching this feature. However, the lines cited describe a rear view of a data processing configuration and the various server blades and power supplies, fans, etc. of the system. They do not teach such a feature and do not refer at all to attaching or detaching a CPU board or power supply.

Claim 3 adds the patentable feature that "if either one of the CPU boards, the IO boards or the power sources is down, the system is restored by detaching said down CPU board, down IO board or down power source from said bus and attaching said detached device to said bus again." For the same reasons as discussed above, no reference teaches or suggests this feature. Examiner additionally cites to Col. 5, line 64 through Col. 6, line 52 as teaching this feature. However, the lines cited describe managed subsystems, a switch control circuit, management logic signals, switch logic, etc. It has nothing to do with attaching or detaching a CPU board, power supply, or I/O board and does not teach the unique features of the present invention.

For at least these reasons, the rejection of claims 2 and 3 under 35 U.S.C. 103(a) is improper and should be withdrawn.

Claim 4 teaches that the "control system is restored by detaching said down CPU board from said bus and attaching said detached CPU board to said bus again." For the reasons discussed

above, no reference teaches or suggests this feature. For at least that reason, the rejection of Claim 4 under 35 U.S.C. 103(a) is improper and should be withdrawn.

CONCLUSION

Reconsideration and allowance are respectfully requested.

Respectfully,

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Date 3/14/07